

FIG. 1 PRIOR ART

WHEN [AT] ARE RECEIVED

D7 OF [A]	D7 OF [T]	FORMAT
0	1	7-BIT EVEN-NUMBER PARITY
1	0	7-BIT ODD-NUMBER PARITY
0	0	7-BIT SPACE
1	1	7-BIT MARK

WHEN [at] ARE RECEIVED

D7 OF [a]	D7 OF [t]	FORMAT
1	0	7-BIT EVEN-NUMBER PARITY
0	1	7-BIT ODD-NUMBER PARITY
0	0	7-BIT SPACE
1	1	7-BIT MARK

FIG. 2 PRIOR ART

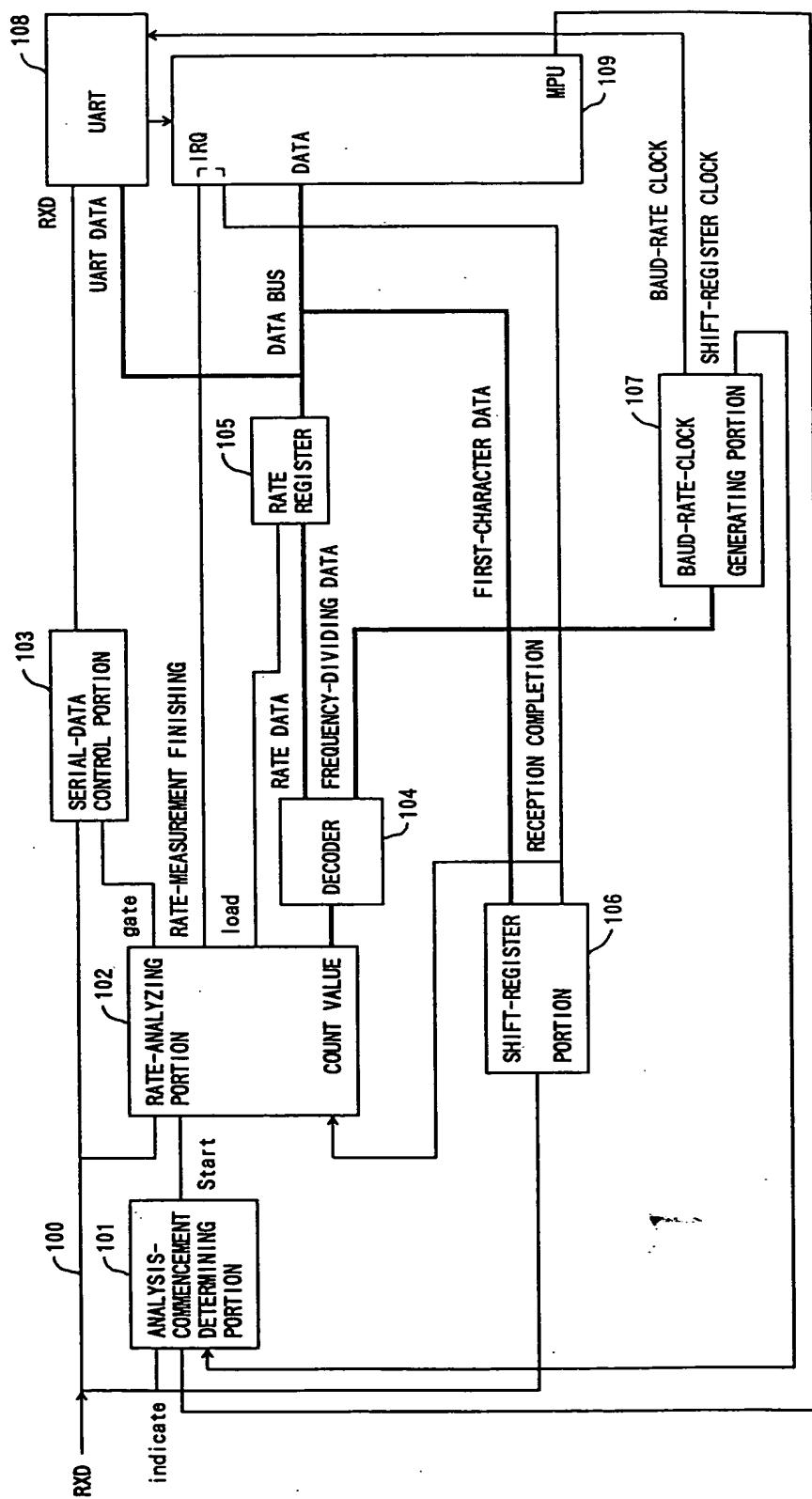


FIG. 3

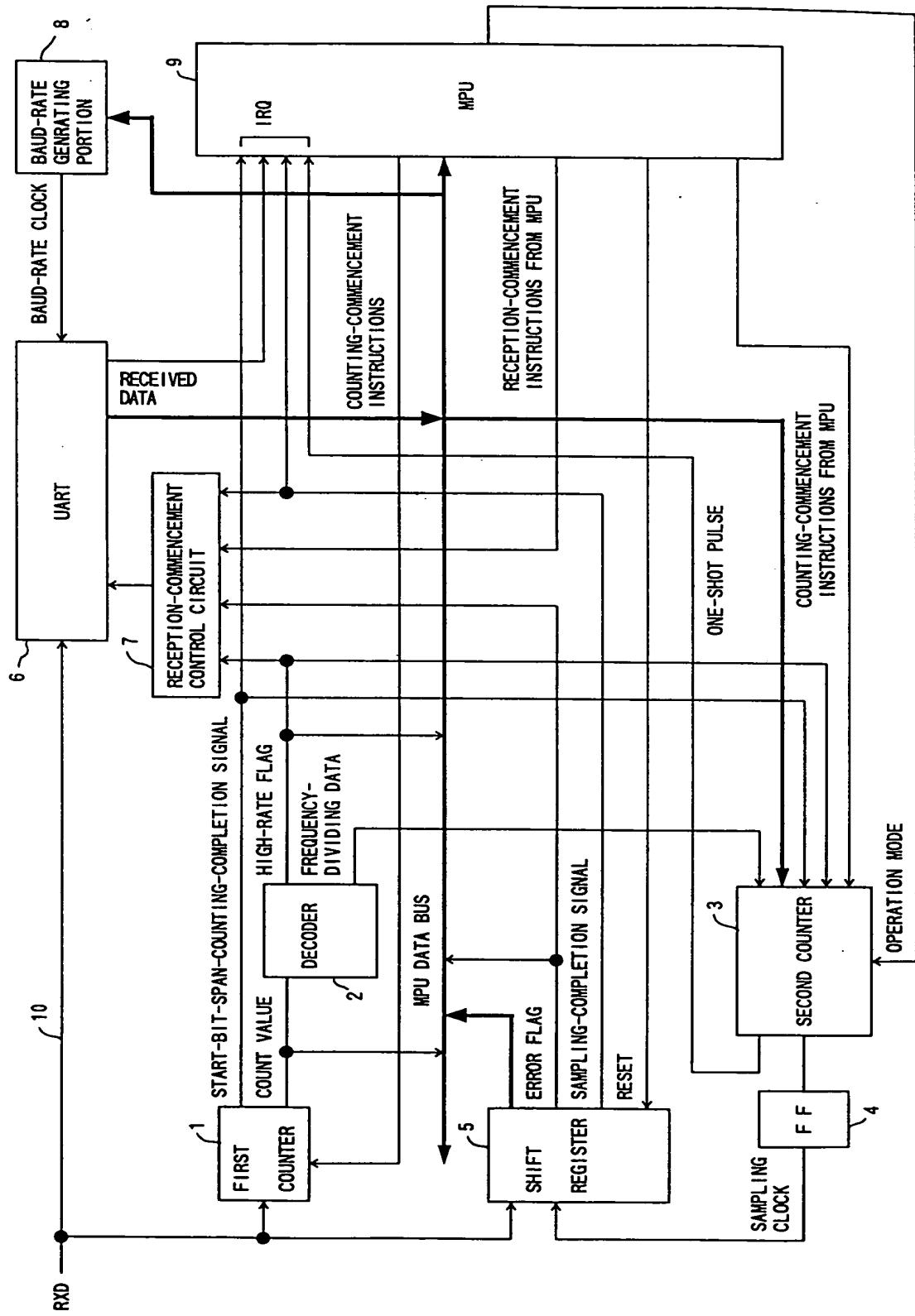


FIG. 4

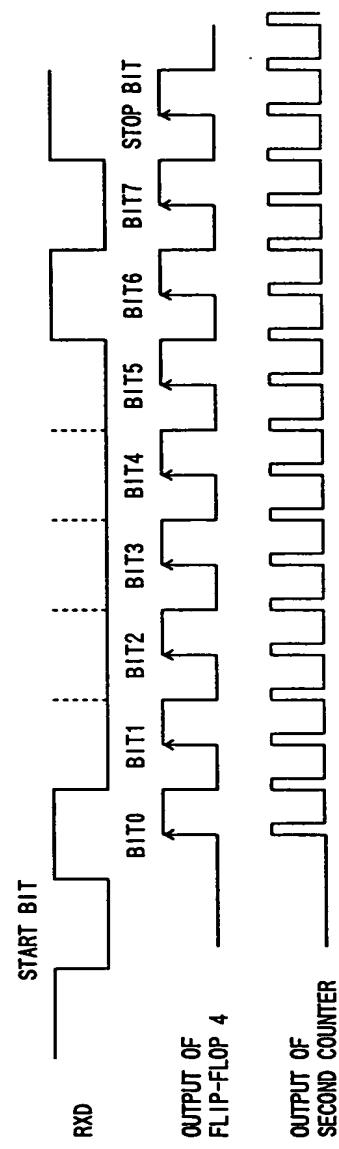


FIG. 5

IN CASE OF NORMAL OPERATION

1. 8432MHz

SECOND COUNTER
(IN A CASE OF 0008)

SECOND-COUNTER CLOCK
(AT EVERY OVERFLOWING)

SECOND-COUNTER CLOCK
(AT EVERY OVERFLOWING)

SAMPLING CLOCK

→ CEND BIT IS SET AND RESULT IS STORED IN SHIFT REGISTER.
IN THIS CASE, RESULT IS 41H.

RxD

BIT0 BIT1 BIT2 BIT3 BIT4 BIT5 BIT6 BIT7

SFTEND BIT

BECAUSE LEVEL OF RXT IS HIGH AT THE TIME OF NINTH PULSE OF SHIFTING CLOCK, SFTEND IS SET. WHEN RXT IS LOW, SFTEND IS NOT SET UNTIL HIGH LEVEL IS SAMPLED AT THE TIME OF ANY OF SUBSEQUENT PULSES OF SHIFT CLOCK

FIG. 6

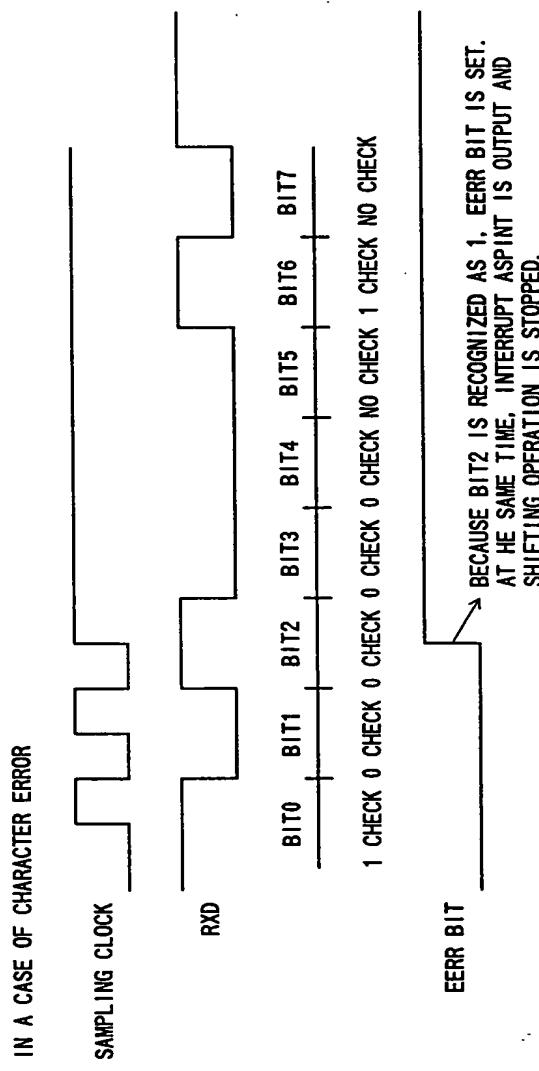


FIG. 7

IN A CASE OF LINE-CHANGE DETECTION

